

Displaying video on a plasma display panel.

The invention relates to a method of displaying a video signal on a plasma display panel as defined in the precharacterizing part of claim 1. The invention further relates to a circuit for displaying a video signal on a plasma display panel as defined in the precharacterizing part of claim 4. The invention also relates to a plasma display device comprising a plasma display panel and a circuit for displaying a video signal on the plasma display panel as defined in the precharacterizing part of claim 5.

In a known Alternate Lighting In Surface Plasma Display Panel (further referred to as ALIS PDP) with  $n$  display lines, each display line comprises a plasma channel with which two spaced-apart select electrodes are aligned. Two consecutive plasma channels have one select electrode in common. The display lines are selected in an interlaced sequence so as to be able to select all display lines of this ALIS PDP one by one. First, during a first display field of display lines, the  $n/2$  odd display lines are selected one by one, then, during a second display field of display lines, the  $n/2$  even lines are selected one by one.

An interlaced video signal has a frame period with a first and a second video field period. Usually, the odd lines of the video signal form the first video field, and the even lines of the video signal form the second video field. When this interlaced video signal has to be displayed on the ALIS PDP, the odd lines of the video signal are displayed on the odd display lines, and the even lines of the video signal are displayed on the even display lines.

When a progressive video signal has to be displayed on the ALIS PDP, two approaches are known, dependent on the number of video lines to be displayed. When the number of video lines to be displayed is substantially equal to the number of display lines, the odd lines of the video signal are displayed on the odd display lines. Thus, the even lines of the video signal are not used, and the odd display lines are selected also in periods during which otherwise the even display lines would be selected. When the number of video lines is substantially equal to half the number of display lines, all the lines of the video signal are displayed on the odd display lines only.

In the situation where interlaced video (for example, HDTV) as well as progressive video (for example, SXGA) is displayed on the ALIS PDP, the display of the interlaced video becomes different for the odd and the even display lines.

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It is, inter alia, an object of the invention to reduce the differences in the display of the odd and the even display lines.

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To this end, a first aspect of the invention provides a method of displaying a video signal on a plasma display panel as claimed in claim 1. A second aspect of the invention provides a circuit for displaying a video signal on a plasma display panel as claimed in claim 4. A third aspect of the invention provides a plasma display with a circuit for displaying a video signal on the plasma display panel as claimed in claim 5. Advantageous embodiments are defined in the dependent claims.

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The invention is based on the recognition that the display of progressive video on the odd display lines only, as performed in the prior art, causes the phosphors of the odd display lines to age at a faster rate than the phosphors of the even display lines. According to the invention, the progressive video is alternately displayed on the odd display lines only, or on the even display lines only. In both situations this is done during a certain period of time which is larger than a field period of the video signal. For example, the period of time is one hour. In this way, the phosphors of the odd and even display lines will age substantially equally and the artifacts during display of the interlaced video signal on all display lines decrease.

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In an embodiment of the invention as claimed in claim 2, the number of video lines is smaller than or substantially equal to half the number of display lines. In this way, only a few or no video lines will not be displayed on the display lines.

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In an embodiment of the invention as claimed in claim 3, the period of time during which the video signal is displayed on the odd or even lines only, is sufficiently large to prevent line flicker.

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These and other aspects of the invention will be apparent from and elucidated with reference to the embodiments described hereinafter.

In the drawings:

Fig. 1 shows part of the structure of a known progressively scanned PDP,

Fig. 2 shows part of the structure of the known ALIS PDP,

Fig. 3 shows a block diagram of a circuit for displaying a video signal on the

5 known ALIS PDP, and

Figs. 4 A-D show voltages supplied to the select electrodes of the ALIS PDP to obtain an interlaced scan.

Fig. 1 shows part of the structure of a known progressively scanned PDP with n  
10 display lines  $D_1, \dots, D_n$ . Each display line  $D_i$  comprises a plasma channel  $P_i$  with which two spaced-apart select electrodes  $S_{i1}, S_{i2}$  are aligned. A display line  $D_i$  is selected to prime associated pixels  $C_{ij}$  (see Fig. 3) by supplying a sufficiently high voltage between the two electrodes  $S_{i1}, S_{i2}$ . A line of black matrix material  $B_m$  separates two consecutive plasma channels  $P_i, P_{i+1}$ .

15 Because two select electrodes  $S_{i1}, S_{i2}$  are associated with one plasma channel  $P_i$  only, it is possible to activate neighboring plasma channels  $P_i$  independently. This provides a progressive scan of the plasma channels  $P_i$  whereby the plasma channels  $P_i$  are activated successively one by one. Detailed information on such a PDP panel and the driving thereof can be found in EP-B-0549275, which is herein incorporated by reference.

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Fig. 2 shows part of the structure of the known ALIS PDP. In the ALIS PDP with n display lines  $D_1, \dots, D_n$ , each display line  $D_i$  comprises a plasma channel  $P_i$  with which two spaced-apart select electrodes  $S_i, S_{i+1}$  are aligned. Again, a display line  $D_i$  is selected by supplying a sufficiently high voltage between the two electrodes  $S_i, S_{i+1}$ . Two consecutive  
25 plasma channels  $P_i, P_{i+1}$  have one electrode  $S_{i+1}$  in common. The display lines  $D_i$  are selected in an interlaced sequence to provide a one-by-one selection of all display lines  $D_i$  of this ALIS PDP. First, during a first field of display lines  $D_i$ , the  $n/2$  odd display lines  $D_i$  are selected one by one, then, during a second field of display lines  $D_i$ , the  $n/2$  even display lines  $D_i$  are selected one by one.

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The addressing of the ALIS PDP is elucidated with respect to Fig. 3 and Figs. 4 A-D.

Fig. 3 shows a block diagram of a circuit for displaying a video signal  $V_s$  on the known ALIS PDP 1. The ALIS PDP 1 shown comprises plasma channels  $P_i$  extending in the horizontal direction. Two select electrodes  $S_i, S_{i+1}$  are associated with each plasma channel  $P_i$ . Data electrodes  $D_{aj}$  extend in the vertical direction. Overlapping regions of the plasma channels  $P_i$  and the data electrodes  $D_{aj}$  form display cells or pixels  $C_{ij}$  one of which is indicated by a circle.

It is known to generate the gray scales of the displayed video by driving the PDP in a sub-field mode. During each display field, a number of sub-fields is generated, each sub-field comprising a prime period and a sustain period. During the prime period, a select driver 2 selects the display lines (rows)  $D_i$  one by one to prime the display cells  $C_{ij}$  of the selected row  $D_i$  with data signals  $D_{sj}$ . A data driver 3 which receives the video signal  $V_s$  supplies the data signals  $D_{sj}$  in parallel. During the sustain period, the select driver 2 supplies pulses to all the rows  $D_i$  associated with the active display field. The plasma channels  $P_i$  are ignited a predetermined number of times to generate light from the pixels  $C_{ij}$  primed to do so. The amount of light produced depends on the number of ignitions. Sustain periods with a different number of ignitions are associated with the different sub-fields in a display field period. The amount of light generated during a display field is the sum of the different amounts of light produced during the sub-fields of this display field. The PDP is able to produce gray scales because, during the priming period of each sub-field, it is possible to select whether a certain pixel has to produce light during the subsequent sustain period or not. Each sub-field may comprise an erase period, or the erase period may occur once in a display field. During the erase period, all pixels associated with the display field are erased. Detailed information on the sub-field operation of a PDP can be found in EP-B-0549275.

The timing circuit 4 receives the horizontal and vertical synchronization signals  $S$  of the video signal  $V_s$  to produce the timing signals for the select driver 2 and the data driver 3.

When a progressive video signal  $V_s$  has to be displayed on the ALIS PDP, two approaches are known, dependent on the number of video lines to be displayed. When the number of video lines to be displayed is substantially equal to the number of display lines  $D_i$ , only the odd lines of the video signal  $V_s$  are displayed on only the odd display lines  $D_i$ . Thus, the even lines of the video signal  $V_s$  are not displayed, and the odd display lines  $D_i$  are selected also in periods during which otherwise the even display lines  $D_i$  would be selected.

When the number of video lines is substantially equal to half the number of display lines  $D_i$ , all the lines of the video signal  $V_s$  are displayed on the odd display lines  $D_i$  only. The timing circuit 4 commands the select driver 2 to only select the lines of the odd field of display lines  $D_i$ . The timing circuit 4 may receive information indicating the display mode, or the timing circuit 4 may detect the type of video signal  $V_s$  by evaluating the horizontal and vertical synchronization signal of the video signal  $V_s$ .

According to the invention, the progressive video  $V_s$  is displayed alternately on the odd display lines  $D_i$  only, or on the even display lines  $D_i$  only. In both situations, this is done during a certain period of time which is larger than a field period of the video signal  $V_s$ .

For example, a certain period of time is one hour, or a certain period of time is related to the time the display is active. When the display is switched on to normal operation after it has been switched off or entered a standby mode, the video signal  $V_s$  is displayed on the other field of display lines  $D_i$ . The timing circuit 4 may comprise a timer or a memory device, respectively, to generate the certain period in time. The timing circuit 4 commands the select driver 2 to only select the display lines  $D_i$  of the odd field of display lines, or to only select the display lines  $D_i$  of the even field of display lines.

Figs. 4 A-D show voltages supplied to the select electrodes  $S_i$  of the ALIS PDP to obtain an interlaced scan. In all Figs. 4, voltages are denoted by a number 0, 1, -1, -2 to indicate the polarity and the relative value of the voltage concerned. For the sake of simplicity, an ALIS PDP with only a few select electrodes  $S_i$  ( $S_1$  to  $S_{12}$ ), data electrodes  $D_{aj}$  ( $D_{a1}$  to  $D_{a6}$ ) and display lines  $D_1, \dots, D_{11}$  is shown. The voltages supplied to the odd select electrodes  $S_1, S_3, \dots, S_{11}$  are shown to the left of the PDP. The even select electrodes  $S_2, S_4, \dots, S_{12}$  are interconnected in two groups, the voltages supplied to these groups are shown to the right of the PDP. The data voltages  $D_{sj}$  are shown below the PDP. In a selected display line  $D_i$ , Pixels  $C_{ij}$  which are primed to generate light are indicated by a solid circle, pixels  $C_{ij}$  which are primed to not produce light are indicated by a dashed circle.

Fig. 4A shows the voltages to select display line  $D_4$  during a certain display field. Fig. 4B shows the voltages to select display line  $D_6$  during the same display field. Fig. 4C shows the voltages to select display line  $D_5$  during a succeeding display field, and Fig. 4D shows the voltages to select display line  $D_7$  during this succeeding field.

It is possible to select the display lines  $D_i$  of a certain display field in different ways. As an example, this is explained with respect to Figs. 4A and 4B. All even rows  $D_2, D_4, \dots, D_{10}$  may be selected one by one by first selecting a certain row, let us assume  $D_4$ , in accordance with Fig. 4A. Next, the consecutive even row  $D_6$  is selected as shown in Fig. 4B. Then, the even row  $D_8$  is selected in accordance with Fig. 4A by applying a  $-1$  voltage to select electrode  $S_5$  and a  $-2$  voltage to select electrode  $S_9$ . Next, the even row  $D_{10}$  is selected in accordance with Fig. 4B by applying a  $-1$  voltage to select electrode  $S_7$  and a  $-2$  voltage to select electrode  $S_{11}$ . And so on. This selection scheme has the disadvantage that the voltages on the even select electrodes have to change for every display line  $D_i$ , which causes a large dissipation. This drawback is prevented by first selecting the rows  $D_4, D_8$  in accordance with Fig. 4A and next the rows  $D_2, D_6, D_{10}$  in accordance with Fig. 4B. In the same way, it is possible to select the odd display rows  $D_i$  first in accordance with Fig. 4C and next in accordance with Fig. 4D.

It should be noted that the above-mentioned embodiments illustrate rather than limit the invention, and that those skilled in the art will be able to design many alternative embodiments without departing from the scope of the appended claims. The embodiments describe an ALIS PDP with plasma channels extending in the horizontal direction. Alternatively, the PDP may be rotated through  $90^\circ$ , such that the plasma channels extend in the vertical direction. The plasma channels may be open towards each other, such that a layer of plasma exists. Instead of plasma channels, the PDP may comprise plasma cells.

An aspect of the invention is defined in a method of displaying a video signal  $V_s$  with  $m$  video lines in a video field period on a plasma display panel 1 having  $n$  display lines  $D_i$ . The  $n$  display lines  $D_i$  are selected (2) in an interlaced way to subsequently select a first and a second field of  $n/2$  display lines  $D_i$  to display an interlaced video signal  $V_s$ . For displaying a progressive video signal  $V_s$ , the  $m$  video lines are alternately displayed (3) on the first field of display lines  $D_i$  only, or on the second field of display lines  $D_i$  only, both during respective time periods which are longer than the video field period.

In the claims, any reference signs placed between parentheses shall not be construed as limiting the claim. The word "comprising" does not exclude the presence of other elements or steps than those listed in a claim. The invention can be implemented by means of hardware comprising several distinct elements, and by means of a suitably programmed computer. In the device claim enumerating several means, several of these means can be embodied by one and the same item of hardware.

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